The Examiner requested a more descriptive title, and a new title is substituted. Specifically, the claimed invention is directed to a structure to increase density of MIM capacitors between adjacent metal layers in an integrated circuit.

The Examiner has mentioned the abstract, disclosure, and drawings, but the Examiner makes no specific objections thereto. Accordingly, no changes are being made except to correct reference errors in the specification.

Claims 1-8 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite, the Examiner questioning claim 1 what is meant by "a second capacitor metal plate layer under said second capacitor dielectric layer and over and removed from said first capacitor metal plate layer."

This rejection is respectfully traversed with respect to claim 1 as amended and dependent claims 2-8. Specifically, with respect to Figs. 4A and 4B of the drawing, the second capacitor metal plate layer 89 under the second capacitor dielectric layer 93 is over the first capacitor metal plate layer 92 and extends from the second capacitor metal plate layer 92 as shown in Fig. 4A. The extension of the second capacitor metal plate layer 89 allows connection to the shared electrode 89 of two parallel capacitors.

Accordingly, it is respectfully submitted that claims 1-8 as amended are in compliance with 35 U.S.C. § 112, second paragraph.

Claim 1 has been rejected under 35 U.S.C. § 102(e) as being anticipated by Aitken et al. 6,159,787, the Examiner referring specifically to Fig. 11(O) and 11(N) to show an integrated circuit having a substrate and a plurality of stacked metal layers thereover, the metal layers delineated as interconnections for the integrated circuit, and the capacitor structure between adjacent stacked metal layers.

This rejection is respectfully traversed. While the present invention and the cited Aitken et al. reference both are related to providing a capacitor structure using interdigitated metal layers as capacitor plates, the claimed invention provides the capacitor structure between adjacent stacked metal layers whereas Aitken et al. utilizes six different metal layers in Fig. 11(O) and four metal layers in Fig. 11(N). The invention is directed to providing a **high-density** capacitor structure between adjacent

stacked metal layers in an integrated circuit, which is not shown by Aitken et al. More specifically, with reference to Fig. 4A, the high density capacitor structure is fabricated between the two metal layers M5 and M6. As shown in Fig. 4B, a first dielectric layer 91 is provided over M5 layer 86 and a composite first capacitor plate 92 is formed over and laterally coextensive with the first dielectric layer 91. A second capacitor plate 95 is formed beneath metal layer M6 (not shown in Fig. 4B) with a second dielectric layer 93 under the portion of the selected one of the stacked metal layers M6. The second capacitor metal plate layer 89 under the second capacitor dielectric layer 93 is over and extends from the first capacitor metal plate layer 91 and extends in Fig. 4A to the left via 88 which connects the second capacitor metal plate with portions of metal layers M5, M6 as a contact, and a first via 88 on the right in Fig. 4A connects the first selected stacked metal layer portion M5 and the second selected stacked metal layer portion M6 to form a second terminal of the capacitor structure.

The provision of this multiple capacitor structure between two metal layers provides for a high density capacitor structure. Aitken et al. does not disclose this since Aitken utilizes six metal layers. This is contrary to the **high density** structure disclosed and claimed by applicant.

Accordingly, it is respectfully submitted that the high density capacitor structure between adjacent stacked metal layers as defined by claim 1 is neither shown nor suggested by Aitken et al.

Claim 2 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Aitken et al. in view of applicant's prior art Figs. 1A-3B, the Examiner again stating that Aitken et al. show the features of the claimed invention but fails to show at least one of the first or second stacked metal layers comprises a plurality of stacked, contiguous metal layers of different composition.

This rejection is respectfully traversed for the reasons given above for the patentability of claim 1 over Aitken et al. since claim 2 depends from claim 1. Claim 2 further defines the composition of the stacked metal layers, which is admittedly known from the prior art. However, the high density capacitor structure between adjacent

stacked metal layers as defined by claim 1 and dependent claim 2 is not shown or suggested by Aitken et al.

Claims 3-8 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Aitken et al. in view of Hoshiba 5,506,748, the Examiner noting that Aitken fails to show that the first capacitor dielectric layer and the first capacitor metal plate layer are laterally coextensive. The Examiner refers to Hoshiba for showing a capacitor in a semiconductor integrated circuit where a first capacitor dielectric layer and a first capacitor metal plate layer are laterally coextensive.

This rejection is respectfully traversed for the reasons given above for the patentability of claim 1 from which claims 3-8 depend. The high density capacitor structure between two adjacent stacked metal layers as defined by claim 1 is neither shown nor suggested by Aitken et al. in view of Hoshiba et al.

Since a new title has been substituted which is more descriptive of the claimed high density capacitor structure between adjacent stacked metal layers, since claims 1-8 as amended are in compliance with 35 U.S.C. § 112, second paragraph, and since claims 1-8 are patentable under 35 U.S.C. § 102(e) over Aitken et al. and under 35 U.S.C. § 103(a) over Aitken et al. in view of applicant's prior art and in view of Hoshiba, all as above set forth, it is requested that claims 1-8 as amended be allowed and the case advanced to issue.

Should the Examiner have any question concerning the present amendment and response, a telephone call to the undersigned attorney is requested.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Page 1, line 1, change the title to read --Structure **[and Method]** to Increase Density of MIM Capacitors **[in Damascene Processes]** Between Adjacent Metal Layers in an Integrated Circuit--

Page 5, lines 11-16, change the paragraph to read:

--Nor are the results improved using more modern damascene processes for the metallization layers of the integrated circuit. Fig. **[2A]** 3A illustrates a current MIM capacitor structure in a integrated circuit manufactured by an exemplary damascene process with the advantage of requiring only one additional masking step. Again, only the details of the metallization layers forming parts of the capacitor structure are described and the capacitor structure which is encircled by a dotted line is shown in greater detail in Fig. **[2B]** 3B.--

Page 5, lines 30 through page 6, line 2, change the paragraph to read:

--The MIM capacitor structure is created by a capacitor dielectric layer 62 on a portion of the M5 metal layer 56 and a capacitor metal layer 63 on the capacitor dielectric layer 62. A metal via 59 connects the capacitor metal layer 63 to the M6 metal layer 60. The details of the capacitor structure is shown in greater detail in Fig. **[1B]** 3B. Note that the M5 metal layer 56 is formed by a Cu layer 56B surrounded by a Ta layer 56A. The capacitor metal layer 63 is a stacked sandwich structure of TiN/AlCu/TiN or Ta/Cu/Ta for the metal layers 63A-63C.--

Page 6, line 22 through page 7, line 14, change these two paragraphs to read:

--The capacitor structure of which the M5 metal layer 86 is a part is encircled by a dotted line and shown in greater detail in Fig. 4B. A first capacitor dielectric layer 91 is placed on a portion of the M5 metal layer 86 and a first metal capacitor plate layer 92 on the dielectric layer 91. Below a portion of the M6 metal layer 90 above the first capacitor dielectric layer 91 and first metal capacitor plate layer 92 is a second metal capacitor plate layer 95 and a second capacitor dielectric layer 93. A metal via 89 separates (and connects) the first metal capacitor plate layer **[91]** 92 and the second capacitor dielectric layer 93. Fig. **[4A]** 4B illustrates the composition of some of the elements of the capacitor structure in greater detail. The M5 metal layer 86 is formed by a barrier metal layer 86A of Ta around a Cu metal layer 86B. The first capacitor dielectric layer 91 (and second capacitor dielectric layer 93) is formed by deposited SiO_2, SiON or SiN. The first metal capacitor plate layer 92 (and second metal capacitor plate layer 95) is a tripartite sandwich structure of metal layers 92A-92C (and 95A-95C) of TiN/AlCu/TiN or Ta/Cu/Ta. The via 89, like the other vias in the metallization interconnection of Fig. 4A is Cu or W.

The MIM capacitor structure forms two capacitors C_1 and C_2 as represented in Fig. **[5A]** 5B. The bottom capacitor C_1 is connected to the M5 metallization layer 86 and the top capacitor C_2 is connected to the M6 metallization layer 90. The via 89, which is actually part of the capacitor structure, connects the two capacitors C_1 and C_2. Structurally it should be noted that in Fig. 4A a right side via 88 connects the M5 metal layer 86 which has a portion covered by the first dielectric layer 91 to the M6 metal layer 90 which has a portion which covers the second metal capacitor plate layer 95. The via 89 connects to M5 and M6 metal layers 86, 90 which are not part of the capacitor structure. To ensure that connection the via 89 is also connected to a via 88 on the left side of the Fig. 4A drawings. Electrically the two capacitors C_1 and C_2 form a circuit shown in Fig. 5B. In other words, if the two capacitors C_1 and C_2 have equal capacitance, the capacitor density is doubled. In the same occupied area, the capacitance is doubled.--